TX Mainboard 7
Hardware Documentation

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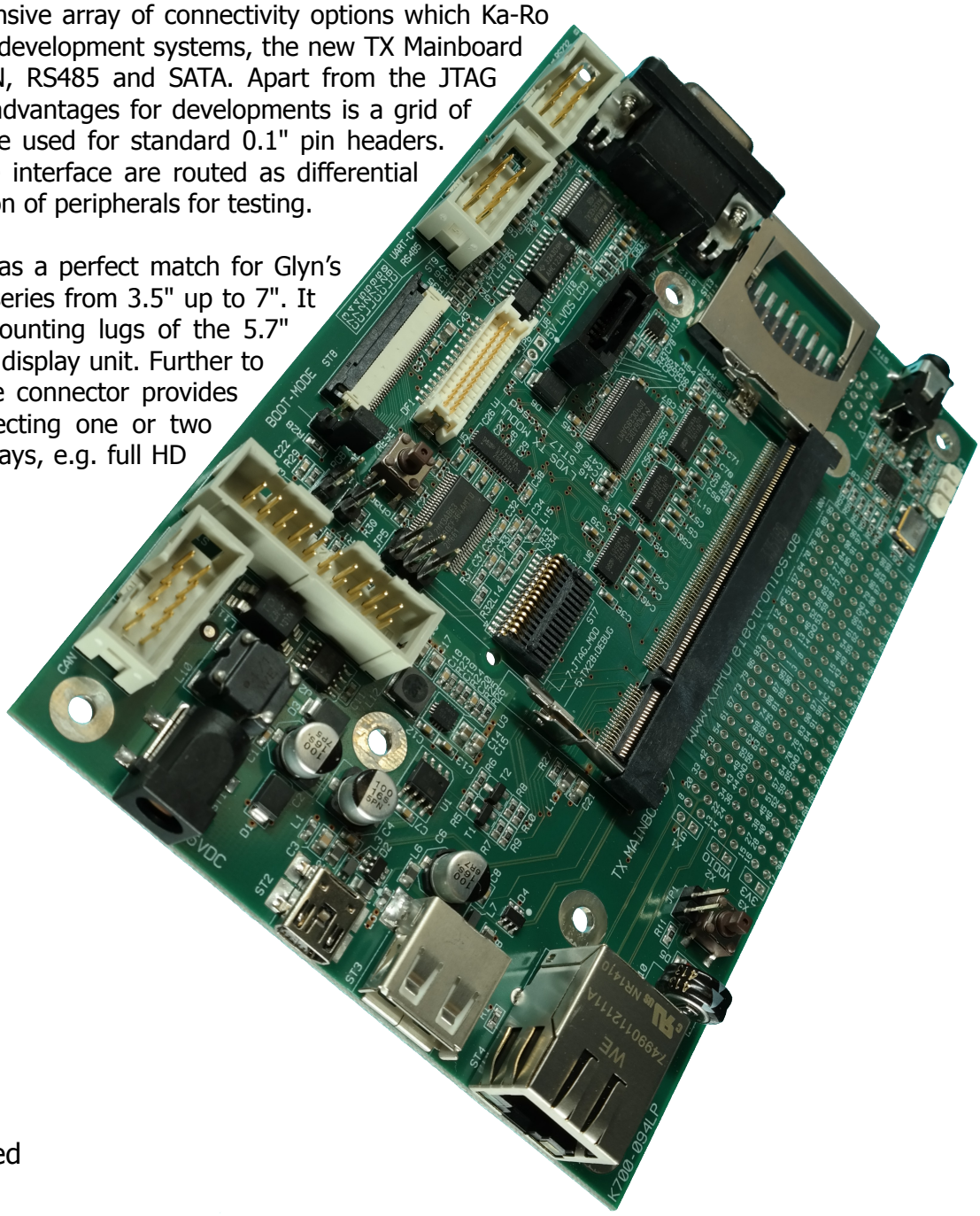
1 Introduction

The Ka-Ro TX Mainboard 7 is an advanced development system, especially designed for building applications based on Ka-Ro's family of TX Computer on Modules.

In addition to the comprehensive array of connectivity options which Ka-Ro has offered in the past in its development systems, the new TX Mainboard 7 now also comes with CAN, RS485 and SATA. Apart from the JTAG connector, one of the main advantages for developments is a grid of test points which can also be used for standard 0.1" pin headers. The signals of the TX6 PCIe interface are routed as differential pairs, thus allowing connection of peripherals for testing.

The TX Mainboard 7 serves as a perfect match for Glyn's TFT Family Concept display series from 3.5" up to 7". It can be screwed onto the mounting lugs of the 5.7" display, thus forming a panel display unit. Further to this, a standard DF13 Hirose connector provides an LVDS interface for connecting one or two larger, higher resolution displays, e.g. full HD panels.



Connectivity

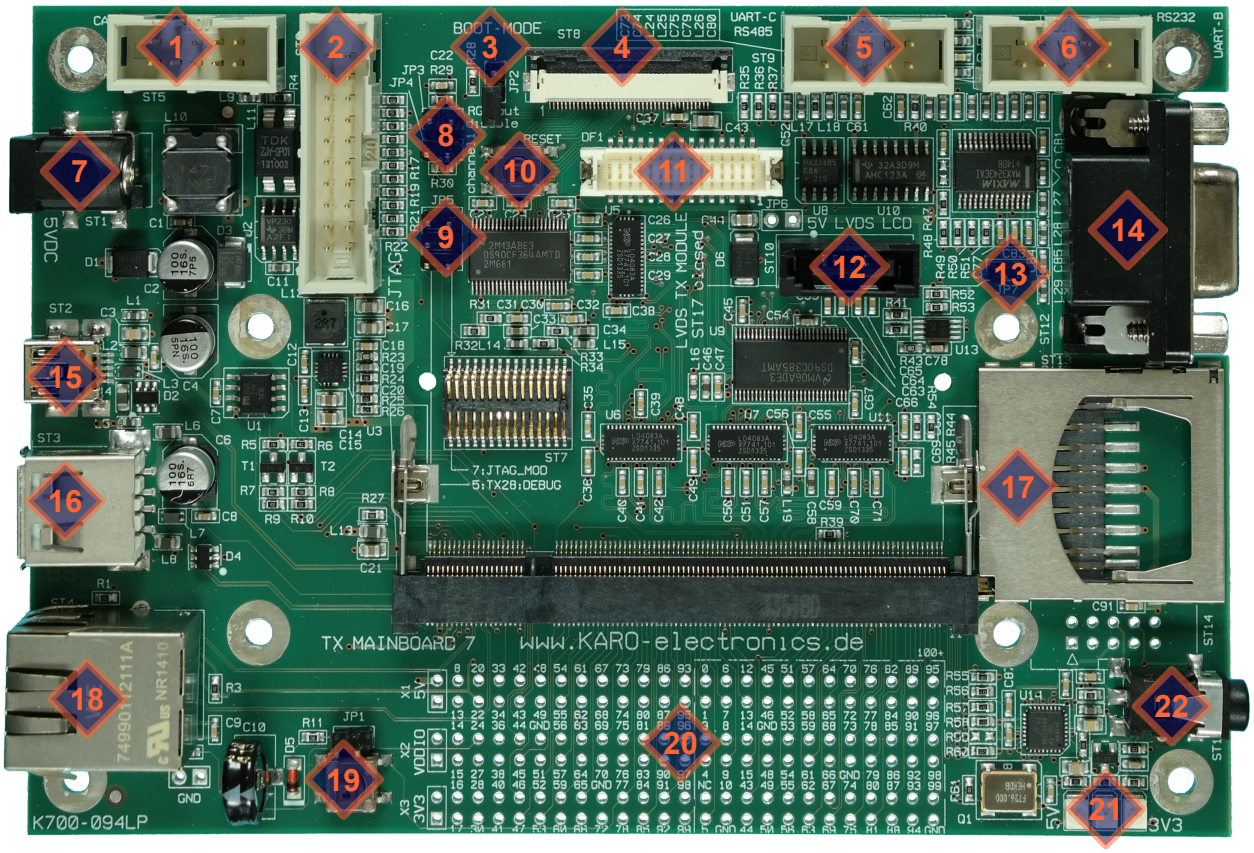
- Ethernet
- USB
- CAN
- RS485
- RS232
- Audio
- SATA
- SD-Card
- Dual LVDS Display
- RGB Display

Development

- JTAG
- Test Pads
- Schematics included

Size and supply

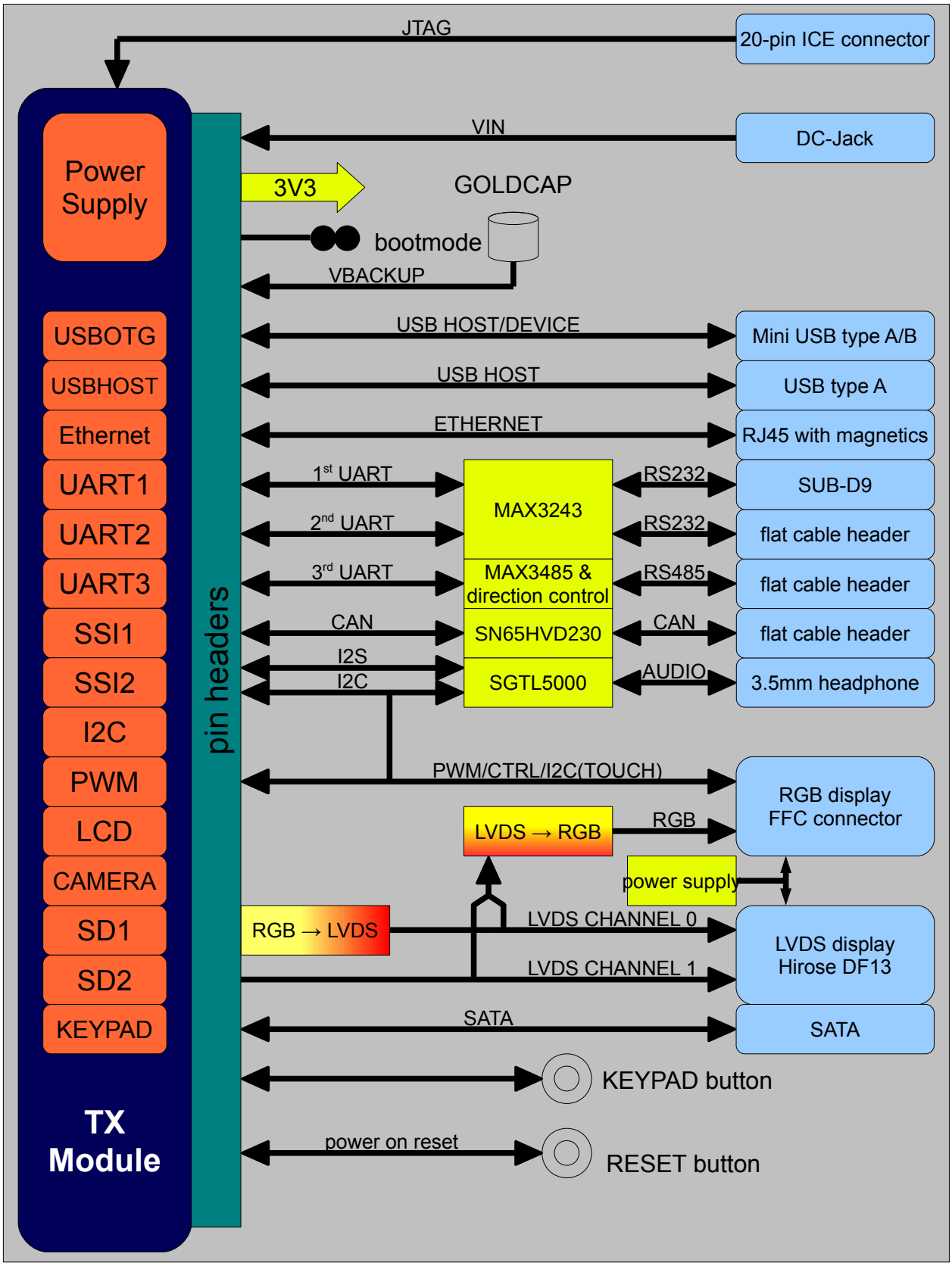
- 5V DC Power supply
- 148mm x 100mm



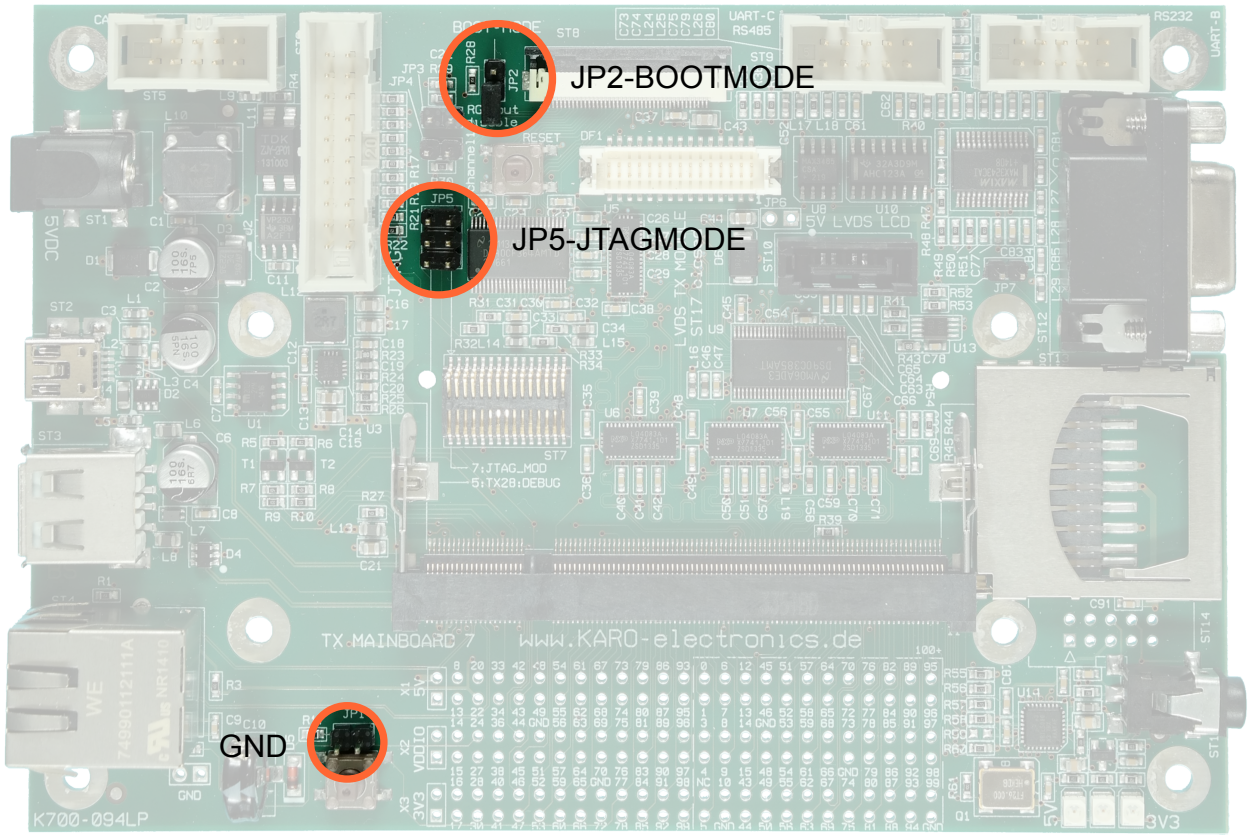
1. CAN
2. JTAG ICE connector
3. BOOTMODE jumper
4. RGB Display
5. RS485 - 3rd UART
6. RS232 - 2nd UART
7. Power supply input
8. RGB Display config jumper
9. JTAG mode jumper
10. RESET button
11. LVDS Display
12. SATA
13. TX RGB/LVDS jumper
14. RS232 - 1st UART
15. Mini A/B USB-Device
16. USB-Host
17. SD-Card
18. Ethernet
19. User button
20. debug headers
21. Status LEDs
22. Audio

2 Hardware

2.1 Blockdiagram



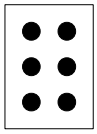
2.2 Jumper



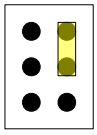
2.2.1 JP2-BOOTMODE

closed	Boot from USB/UART
open	Boot from NAND (default)

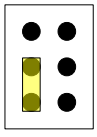
2.2.2 JP5-JTAGMODE



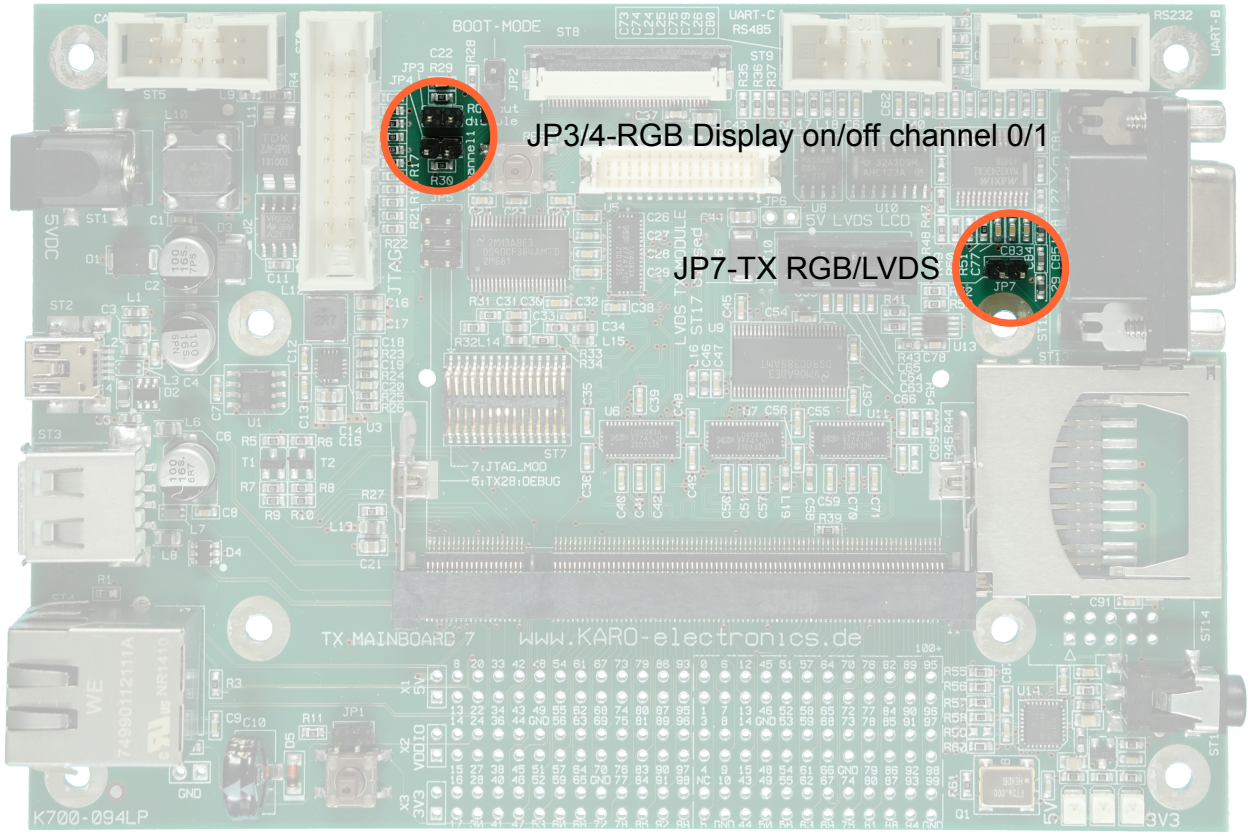
Default
TX28 – DEBUG = H
TX53,TX6 – JTAG_MOD = L



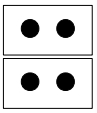
TX53,TX6 – JTAG_MOD = H



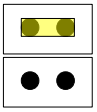
TX28 – DEBUG = L



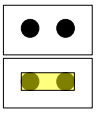
2.2.3 JP3/4 RGB Display disable and channel select



Channel 0 (Default)
LVDS → RGB display enabled
connected to LVDS channel 0
100 Ohms termination on LVDS channel 0



Disable
LVDS → RGB display disabled
No termination



Channel 1
LVDS → RGB display enabled
connected to LVDS channel 1
100 Ohms termination on LVDS channel 1

2.2.4 JP7 – TX RGB/LVDS

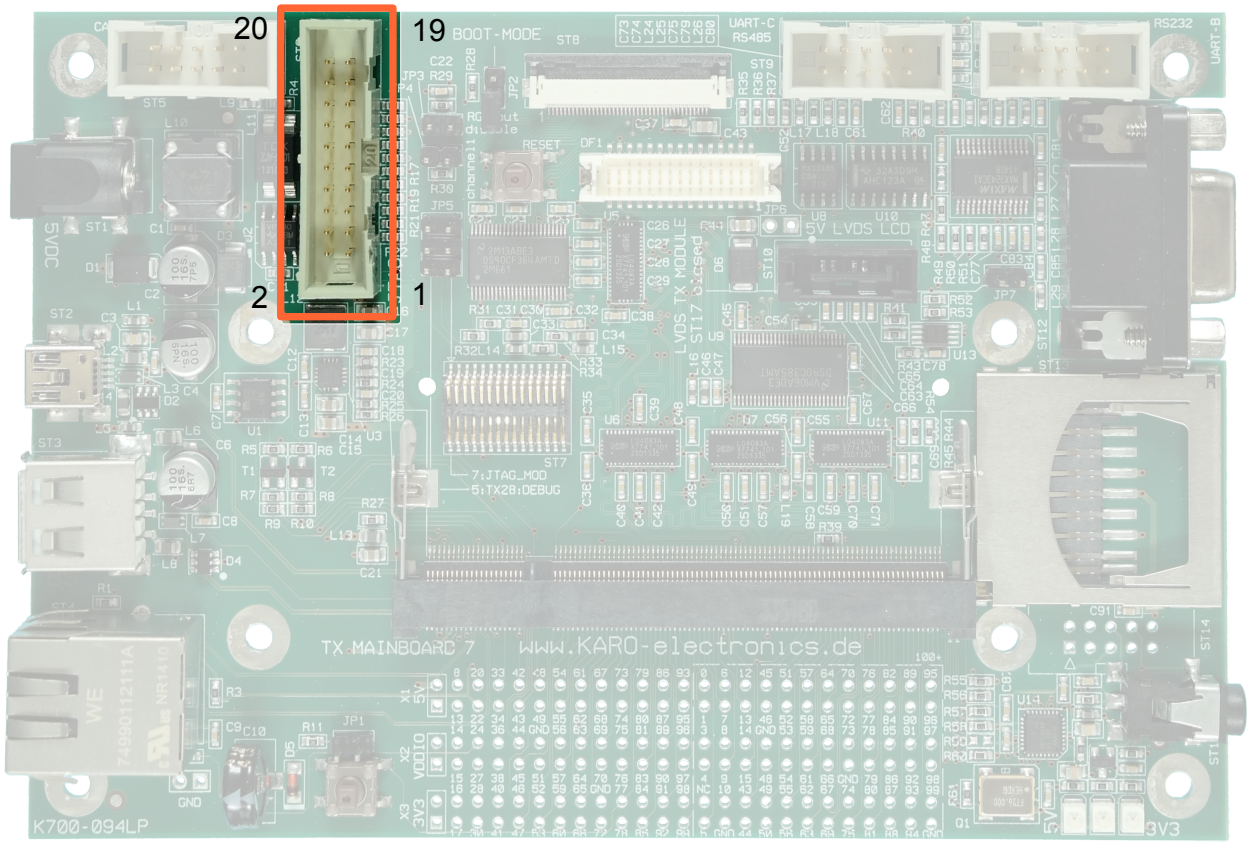
RGB (Default)
Standard TX module

LVDS
LVDS TX module

2.3 Pin Description

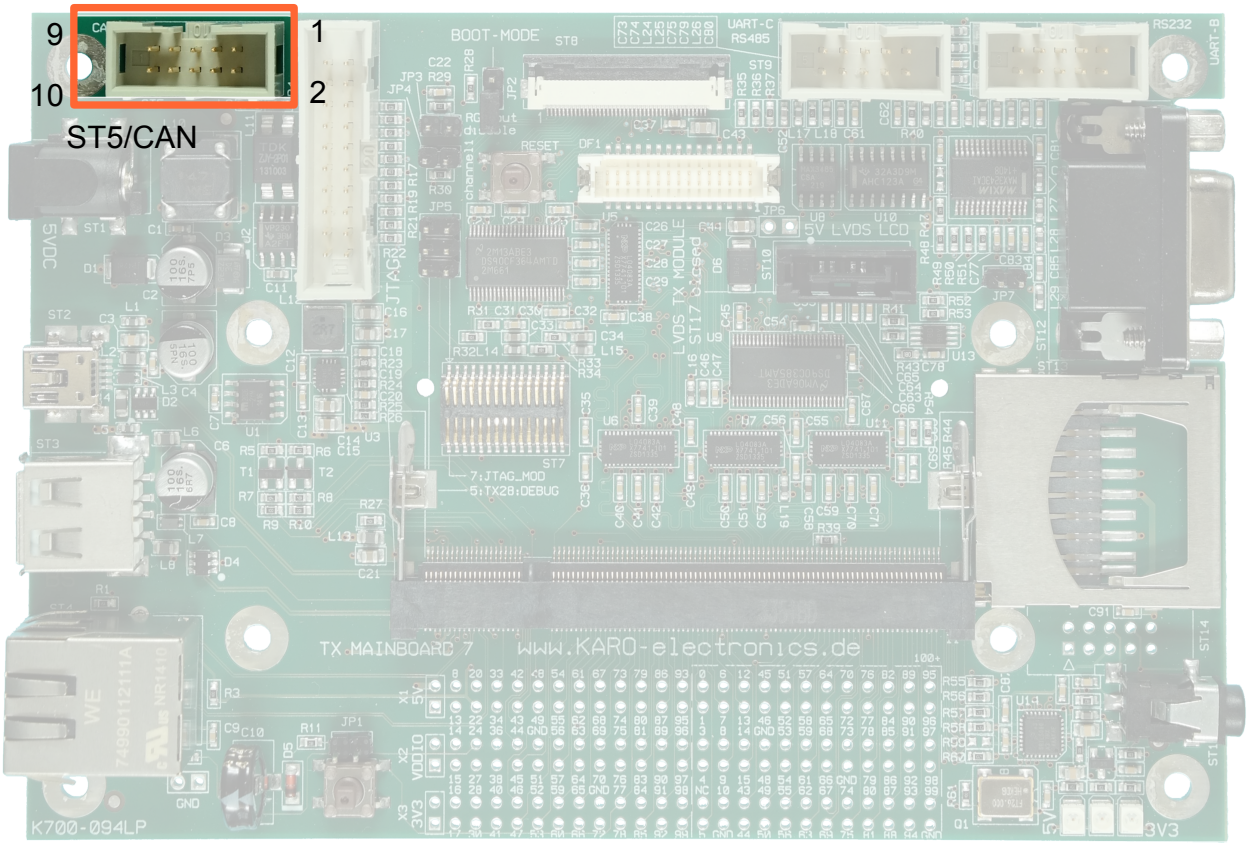
For information about the DIMM pinout, please refer to the TX module datasheet.

2.3.1 ST6 JTAG ICE Interface



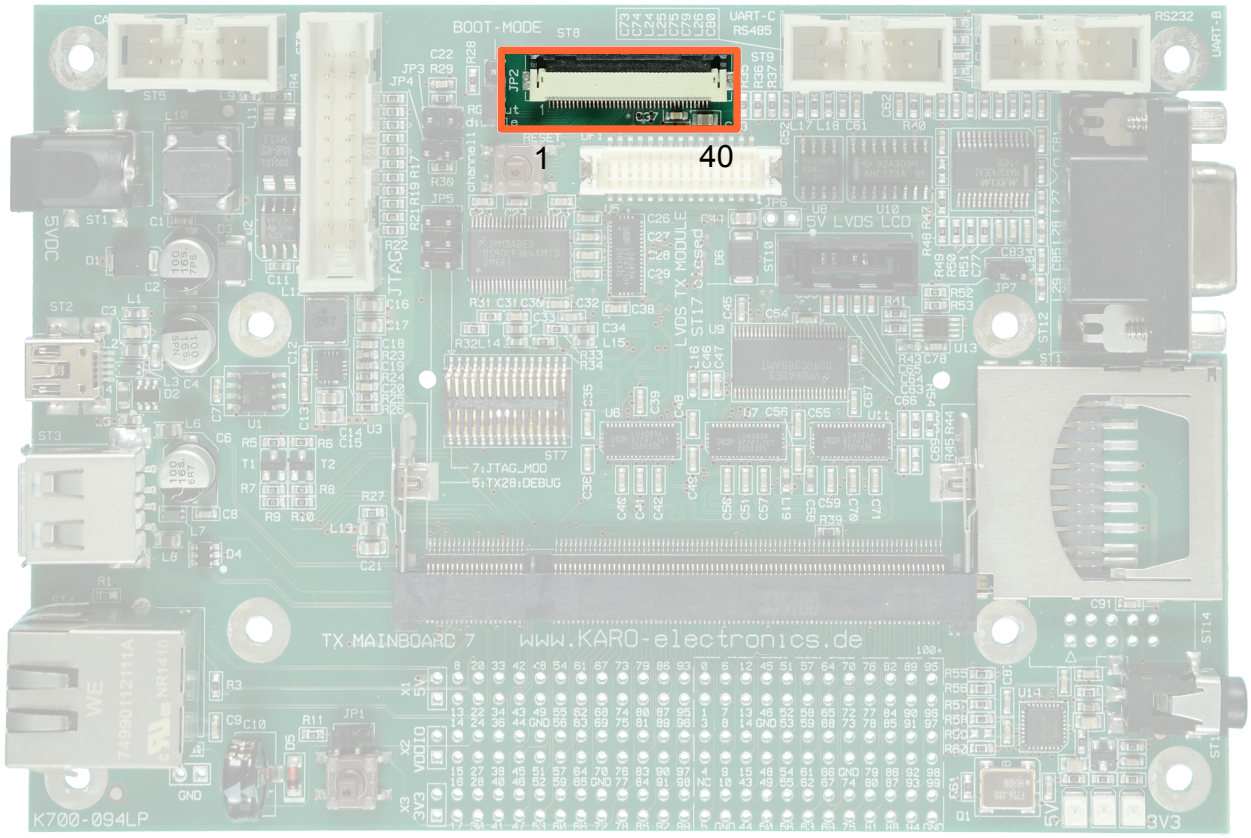
Name	Pin #		Name
3V3	1	2	3V3
TRST#	3	4	GND
TDI	5	6	GND
TMS	7	8	GND
TCK	9	10	GND
RTCK	11	12	GND
TDO	13	14	GND
SRESET#	15	16	GND
not connected	17	18	GND
not connected	19	20	GND

2.3.2 ST5 CAN



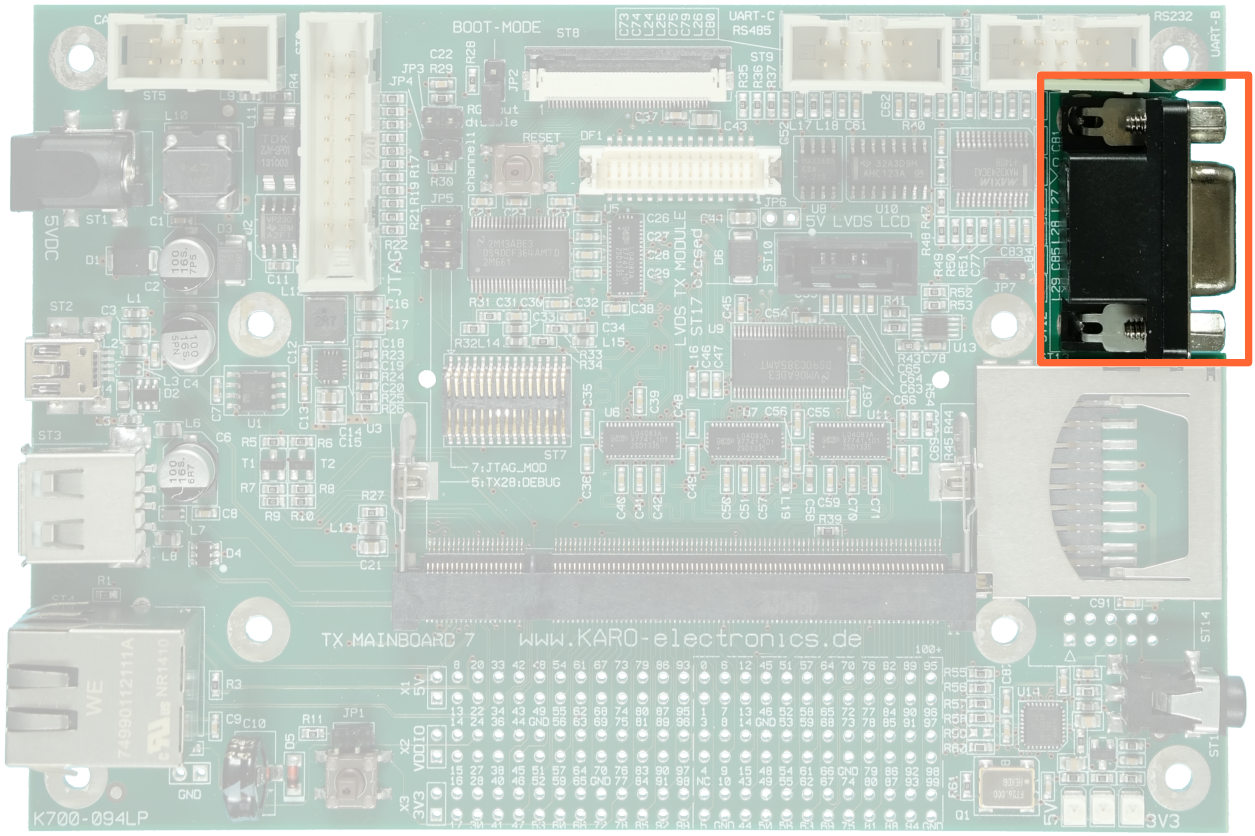
Name	Pin #		Name
not connected	1	2	GND
CAN_L	3	4	CAN_H
GND	5	6	not connected
not connected	7	8	not connected
not connected	9	10	not connected

2.3.3 ST8 Family Concept RGB LCD

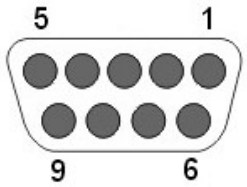


Pin #	Name	Pin #	Name
1	#LCD_RESET/P150	21	LDD[19]
2	#RST/P149	22	LDD[18]
3	LDD[7]	23	GND
4	LDD[6]	24	LSCLK/P146
5	LDD[5]	25	WAKE/P152
6	LDD[4]	26	HSYNC/P143
7	LDD[3]	27	VSYNC/P144
8	LDD[2]	28	OE_ACD/P145
9	GND	29	LCD_ENABLE/P151
10	LDD[15]	30	3V3
11	LDD[14]	31	GND
12	LDD[13]	32	GND
13	LDD[12]	33	3V3
14	LDD[11]	34	3V3
15	LDD[10]	35	#INT/P148
16	GND	36	PWM0/P42
17	LDD[23]	37	SCL
18	LDD[22]	38	not connected
19	LDD[21]	39	SDA
20	LDD[20]	40	not connected

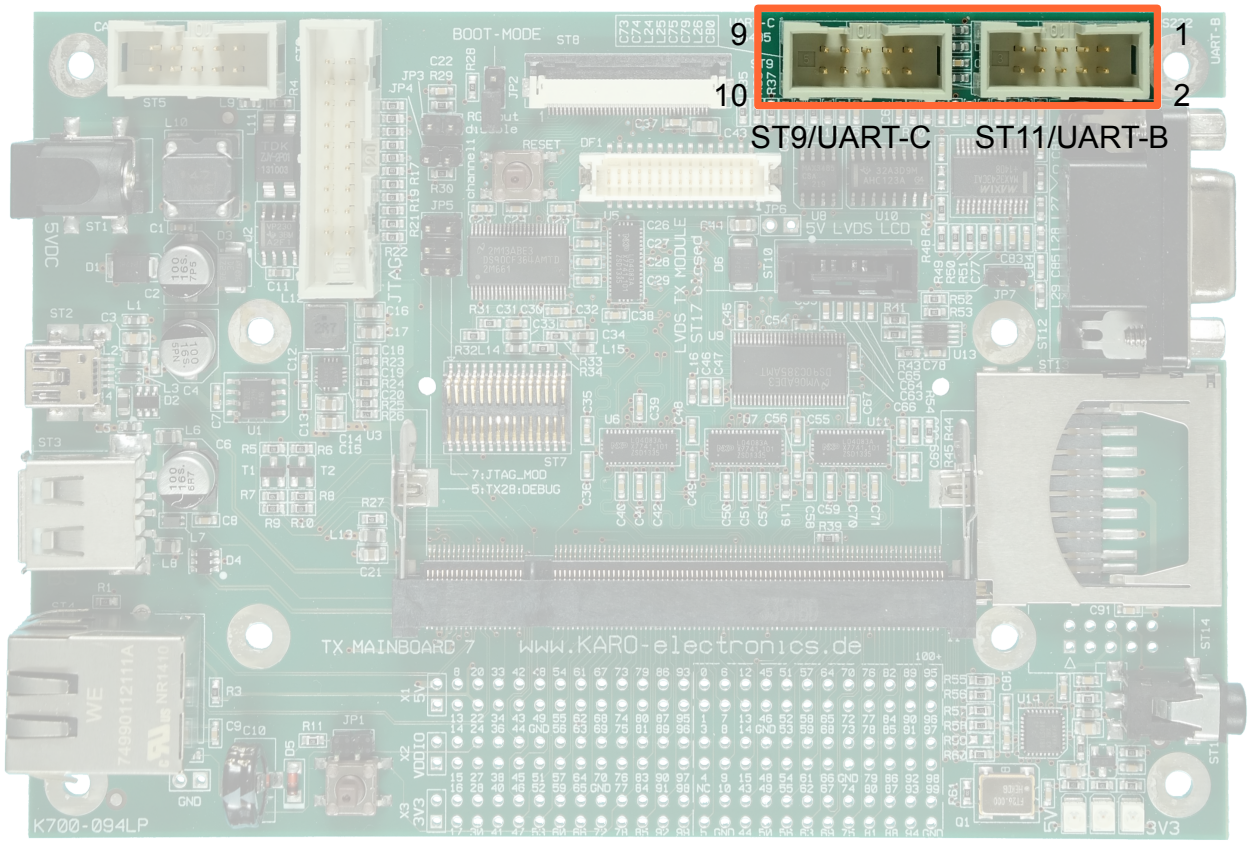
2.3.4 ST12 RS232 (UART-A)



Pin #	Name
1	1-4-6 connected onboard
2	TxD
3	RxD
4	1-4-6 connected onboard
5	GND
6	1-4-6 connected onboard
7	not connected
8	not connected
9	not connected



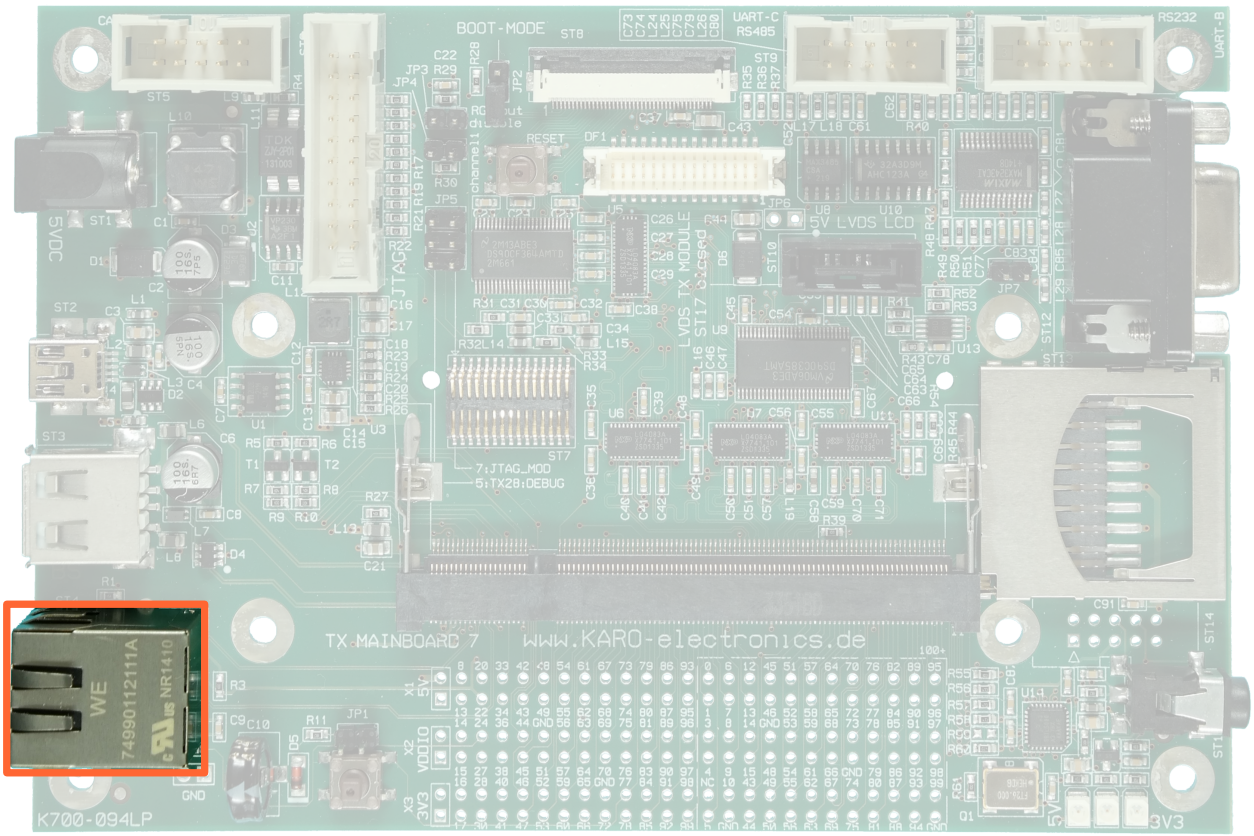
2.3.5 ST9 RS485 (UART-C), ST11 RS232 (UART-B)



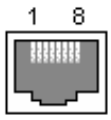
ST11 RS232 (UART-B)			
Name	Pin #		Name
1-2-7 connected onboard	1	2	1-2-7 connected onboard
TxD	3	4	CTS
RxD	5	6	RTS
1-2-7 connected onboard	7	8	not connected
GND	9	10	not connected

ST9 RS485 (UART-C)			
Name	Pin #		Name
not connected	1	2	+5V
not connected	3	4	not connected
B	5	6	A
not connected	7	8	not connected
GND	9	10	not connected

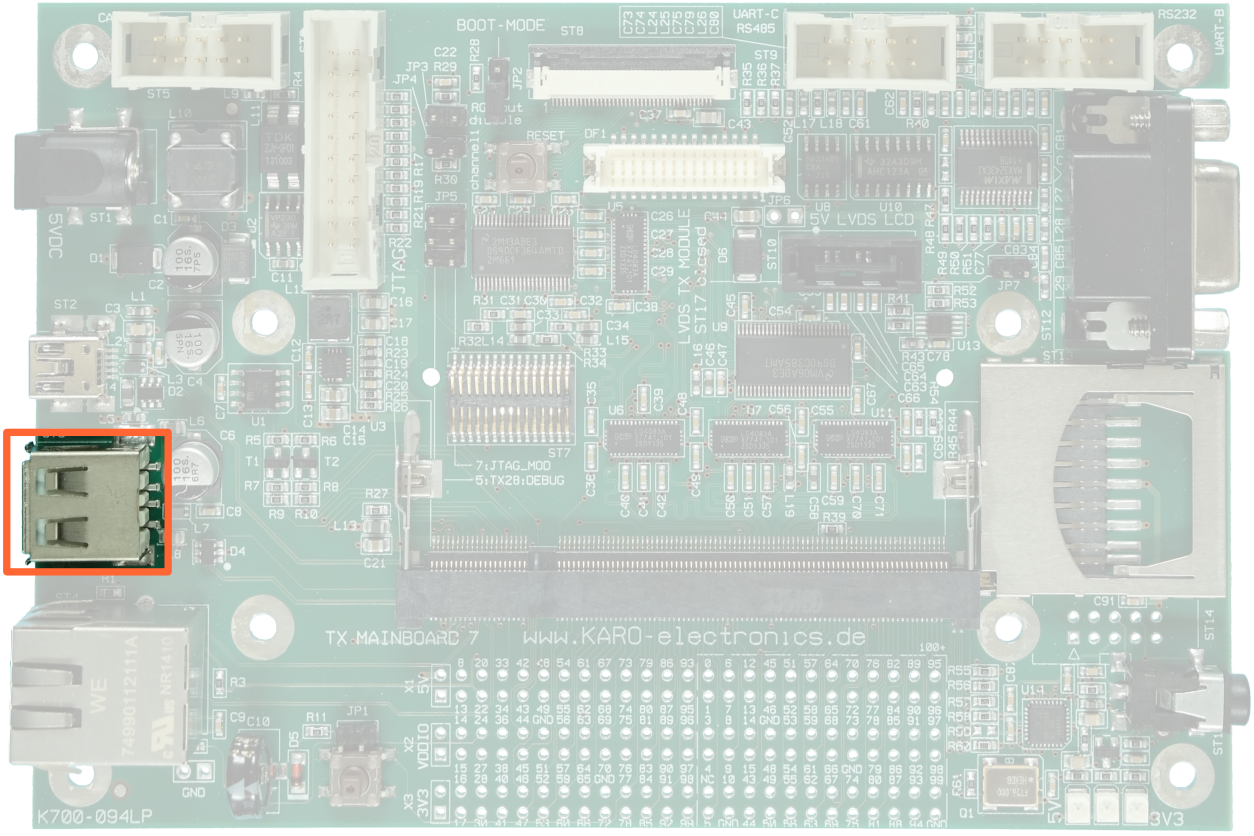
2.3.6 ST4 Ethernet



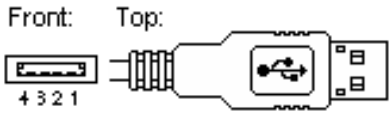
Pin #	Name
1	TX+
2	TX-
3	RX+
4	not used
5	not used
6	RX-
7	not used
8	not used



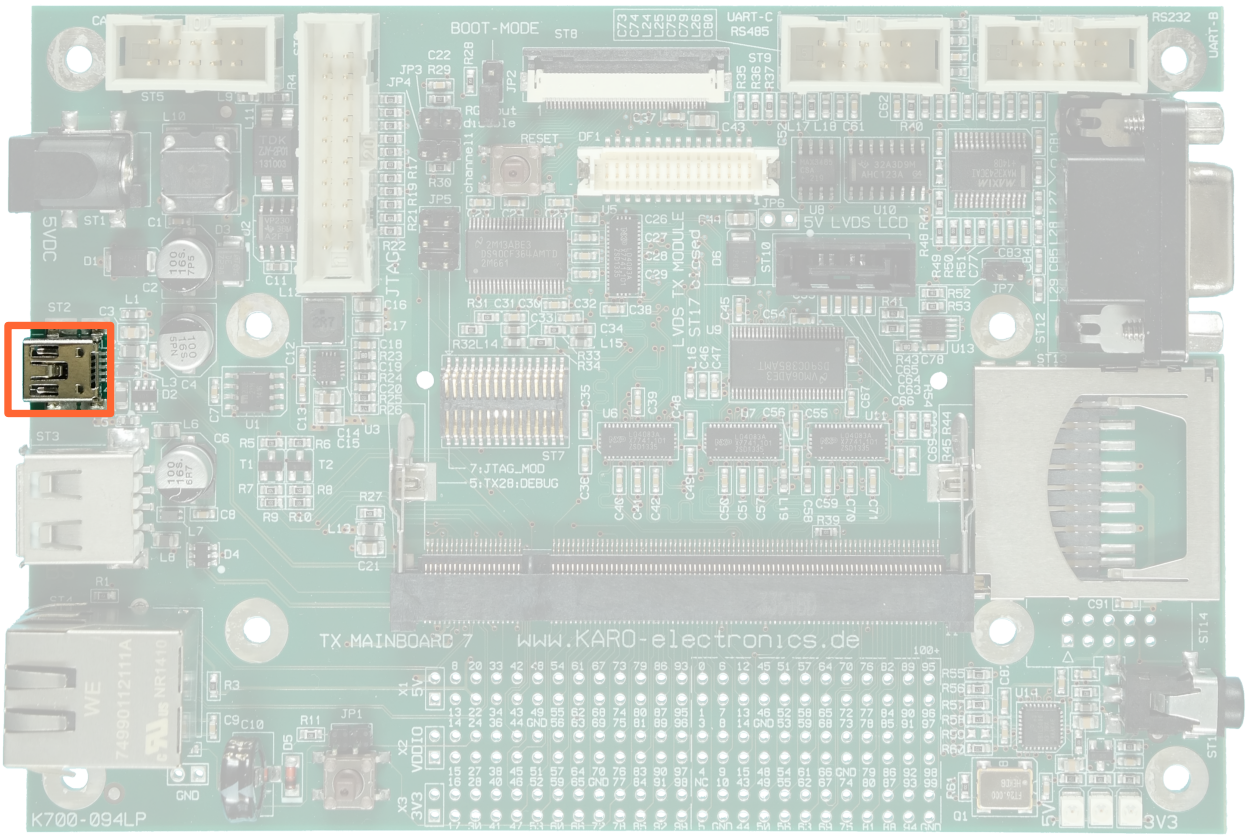
2.3.7 ST3 USB Host Interface



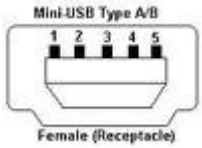
Pin #	Name
1	5V
2	DATA-
3	DATA+
4	GND



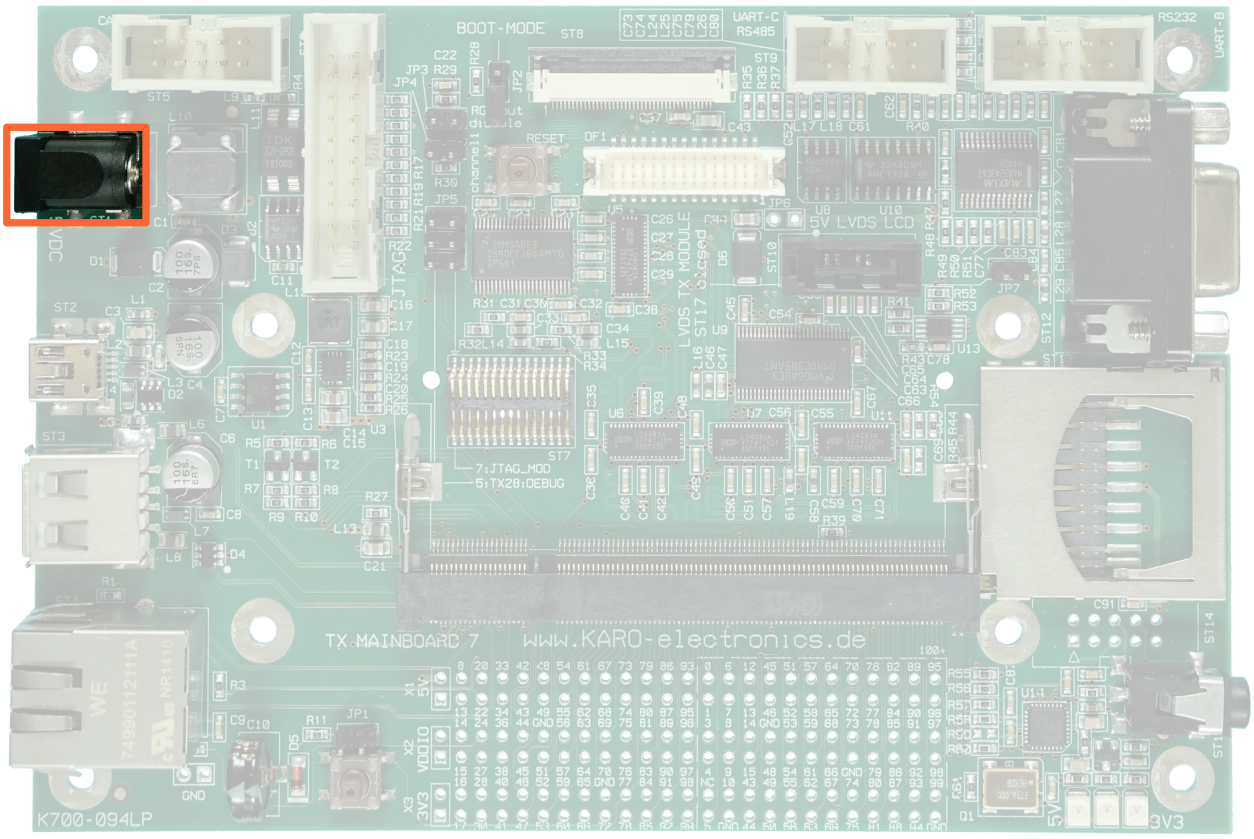
2.3.8 ST2 USB OTG



Pin #	Name
1	5V
2	DATA-
3	DATA+
4	ID
5	GND

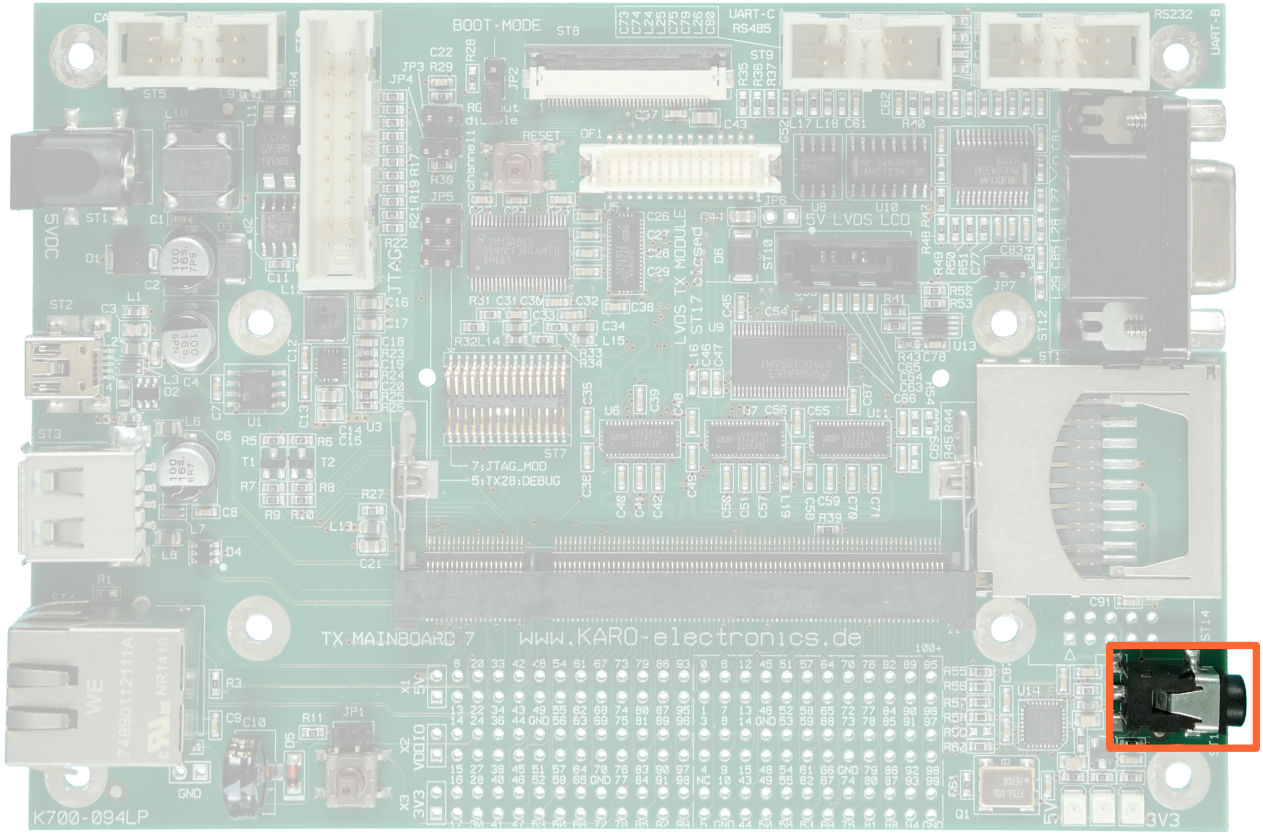


2.3.9 ST1 Power Supply

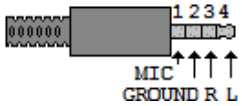


Pin	Name
Inner	3-5VDC
Outer	GND

2.3.10 ST8 Headphone



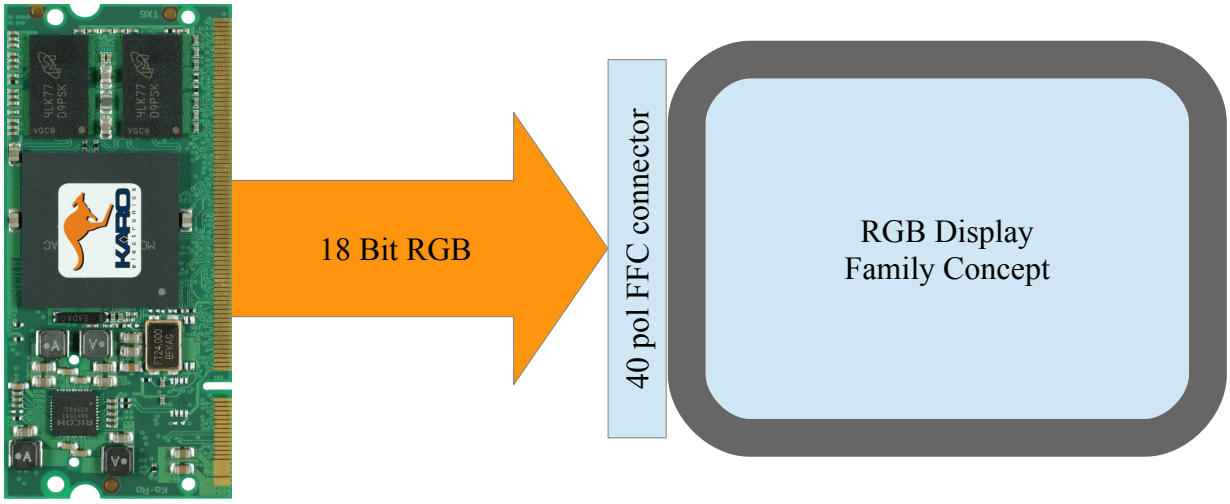
Pin	Function
1	MIC
2	GND
3	Line out right channel
4	Line out left channel



2.4 Display configuration

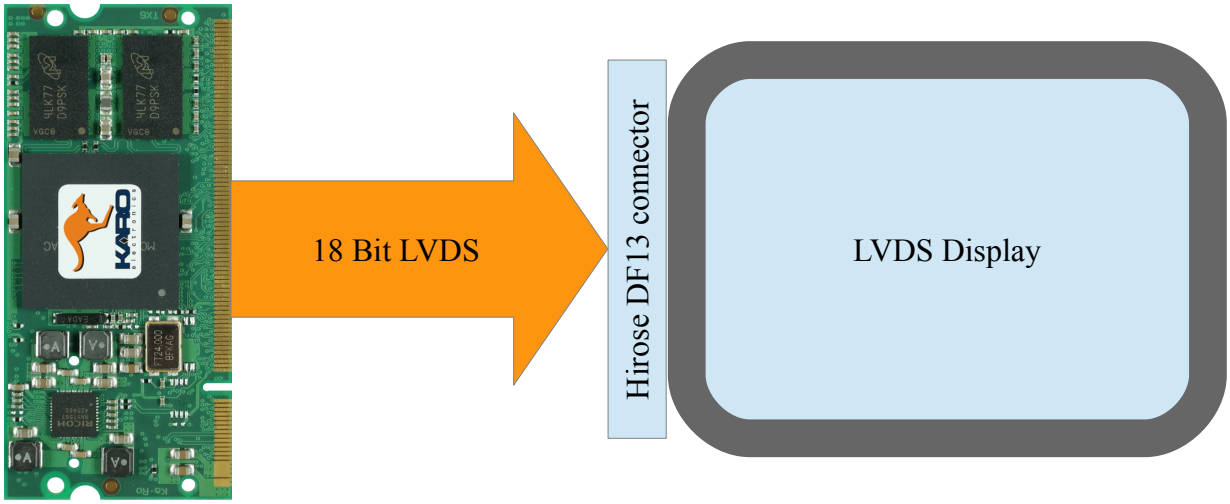
2.4.1 Standard TX module – Family Concept Display

Configuration:	RGB:ON	CHANNEL:0	TX:RGB
	JP3 – open	**JP4 – open**	**JP7 – open**



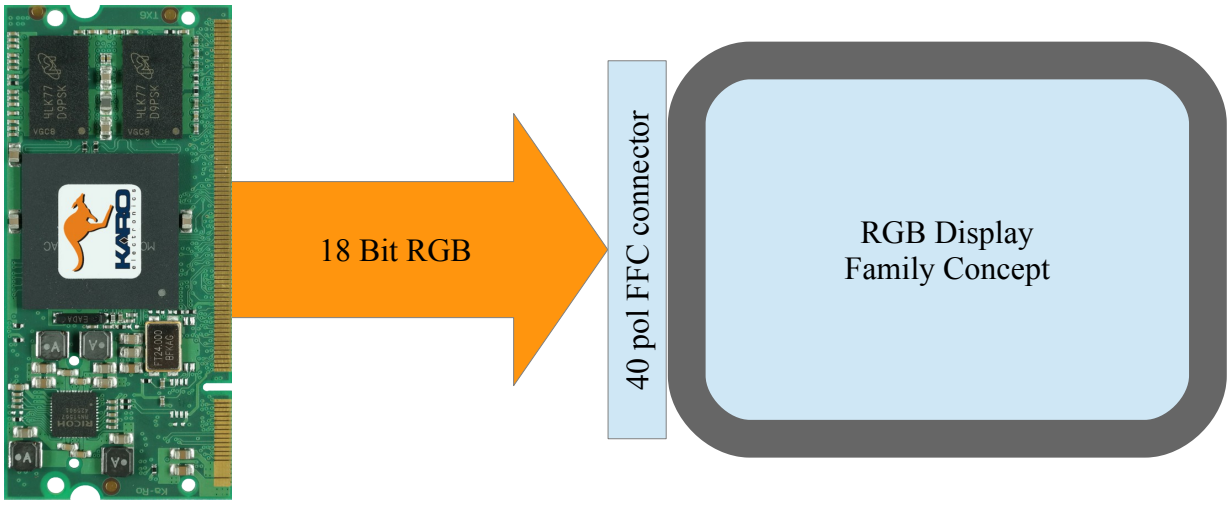
2.4.2 Standard TX module – LVDS Display

Configuration:	RGB:OFF	CHANNEL:0	TX:RGB
	JP3 – closed	**JP4 – open**	**JP7 – open**



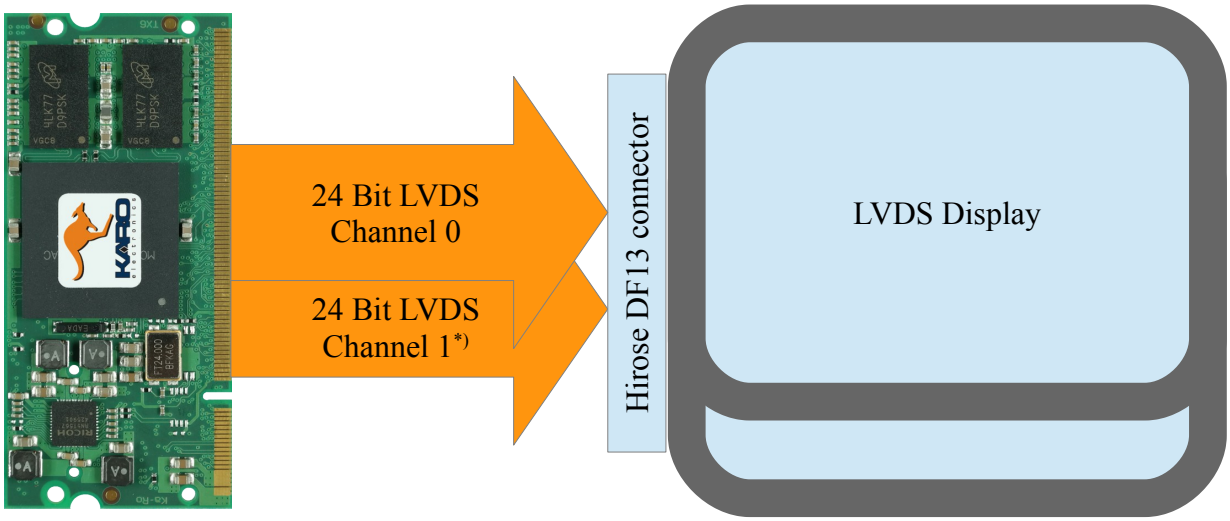
2.4.3 LVDS TX module – Family Concept Display

Configuration:	RGB:ON	CHANNEL:0	TX:LVDS
	JP3 – open	**JP4 – open**	**JP7 – closed**



2.4.4 LVDS TX module – LVDS Display (Dual Channel or Dual Display)

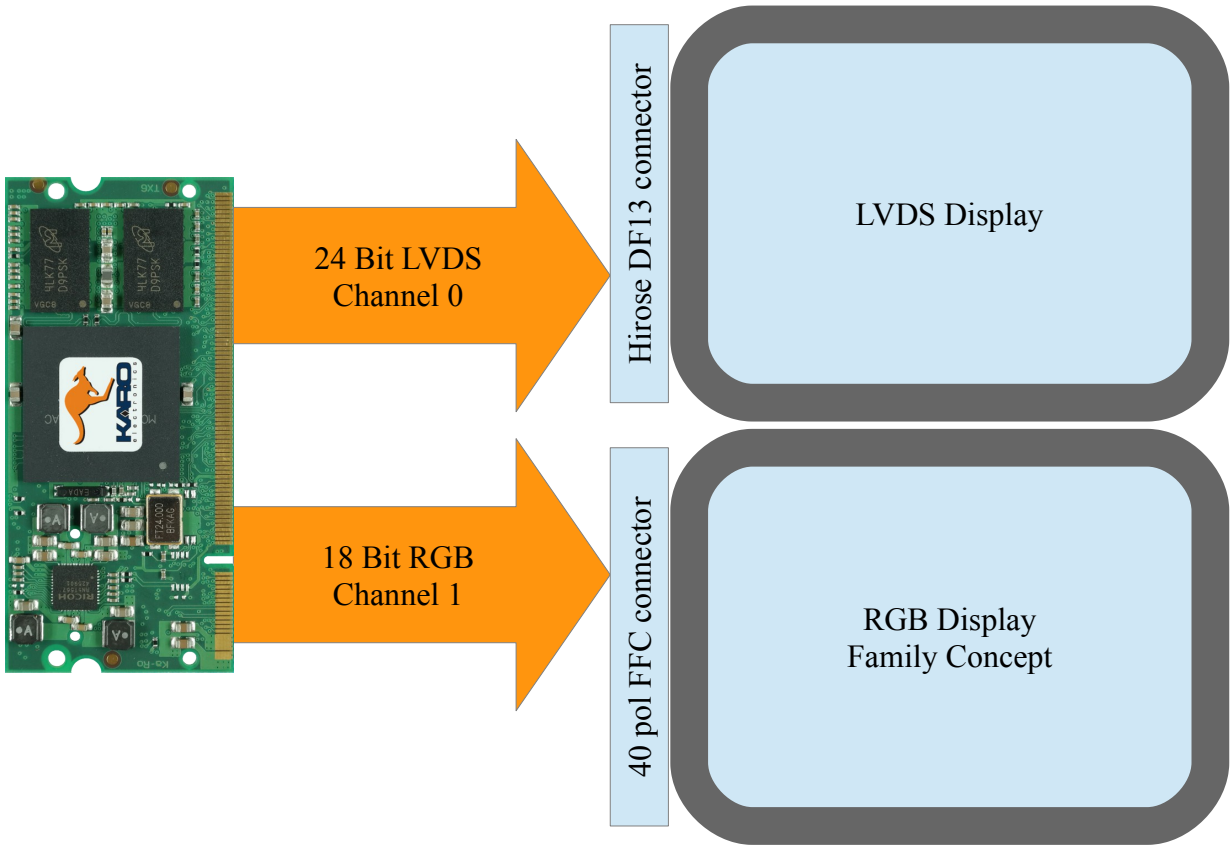
Configuration:	RGB:OFF	CHANNEL:0	TX:LVDS
	JP3 – closed	**JP4 – open**	**JP7 – closed**



*) A disconnected trace of channel 1 has to be joined on TX Mainboard version 7a if needed. Refer to the latest schematics for details.

2.4.5 LVDS TX module – Dual Display – LVDS & Family Concept Display

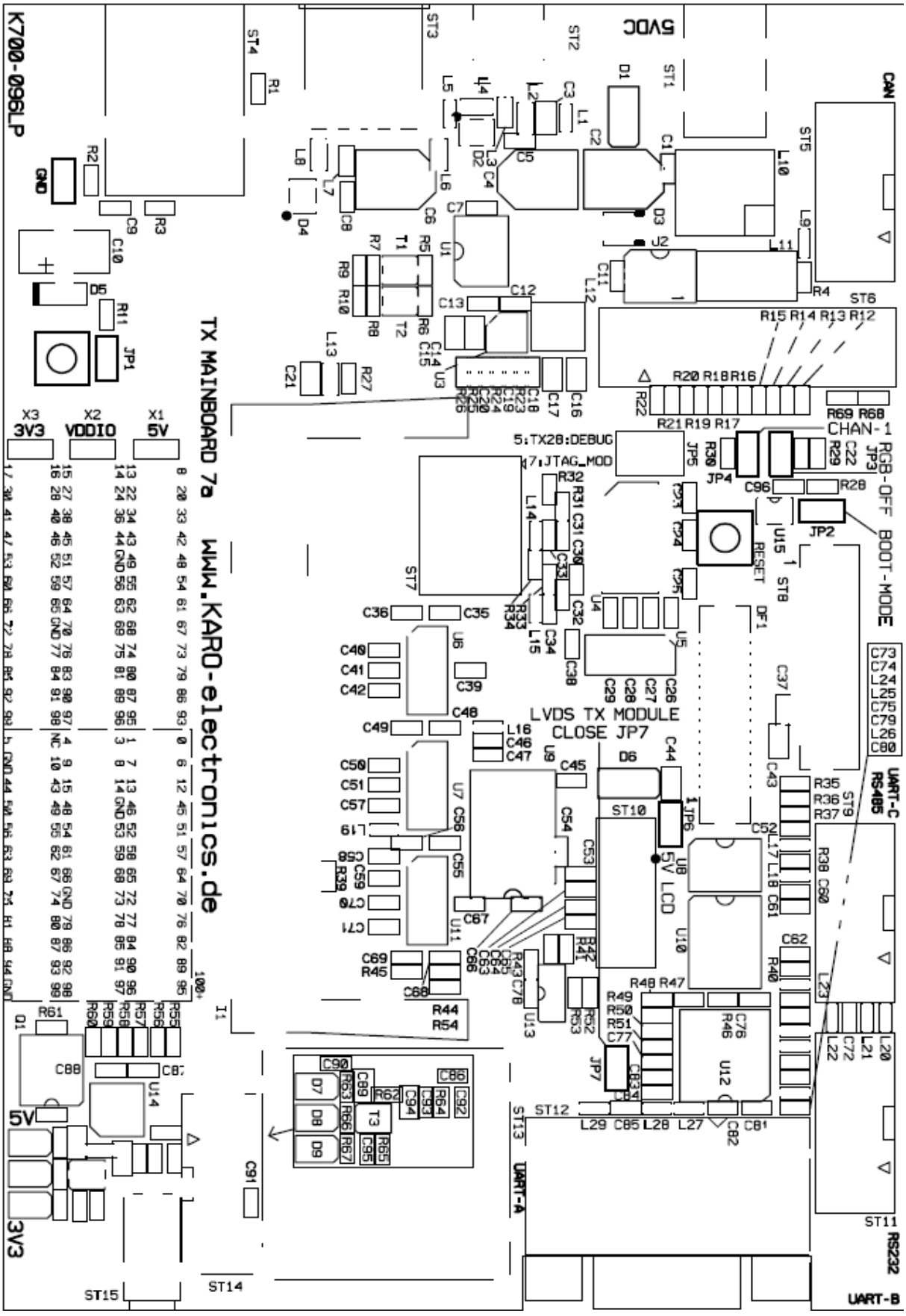
Configuration:	RGB:ON	CHANNEL:1	TX:LVDS
	JP3 – open	**JP4 – closed**	**JP7 – closed**



2.5 24 Bit LVDS remark

There is an issue on TX Mainboard version 7a. LCD[0] (LSB Blue) is missing on a 24-bit LVDS display if a standard RGB TX module is used and the 2nd channel of LVDS TX modules cannot be used because a trace has been disconnected. Refer to the latest schematics for details.

2.6 Component Locations



3 Document revision history

Revision	Changes
2015-04-14	Initial release
2015-04-29	Remarks for TX Mainboard 7a 24 Bit LVDS issue added